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# Introduction

The aim of this lab is to introduce a design flow that allows you to create your own custom Intellectual Property (Custom IP) targeted at a Zynq device using Xilinx’s Vivado 2013.4. The lab has been created for senior undergraduates using the ZedBoard. We assume the student is familiar with the use of VHDL for specifying hardware. The lab explains how to modify the generated component, by focusing on how the AXI-LITE protocol works and how it can be utilised to establish a two-way data flow between the processing system (PS) and the hardware component implemented in programmable logic (PL). This lab concludes on methods for maintaining and integrating this IP as part of a larger design.

Communications Protocol

The following protocol is used in this lab:

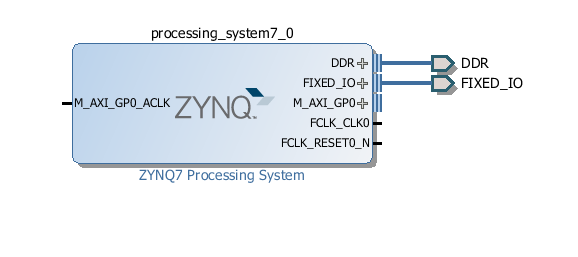


# Configure Highlevel design

For this please refer to lab1 of the Xilinx Advanced Embedded Design course, so you know how to create a Vivado design file with an ARM processor using a GPIO AXI component. In this lab the GPIO AXI component will be replaced by our own custom IP component, which will be programmed on a hardware level (VHDL) to provide the functionality stated in the introduction.

In the end you should have:

* Added a Zynq7 processing system (which has UART1 enabled)
* Applied block automation (without board pre-sets applied) to auto connect the DDR/FIXED\_IO pins to external pins
* Opened up this design on the “Open block diagram view” to show the following



*Figure 0.1: Initial design*

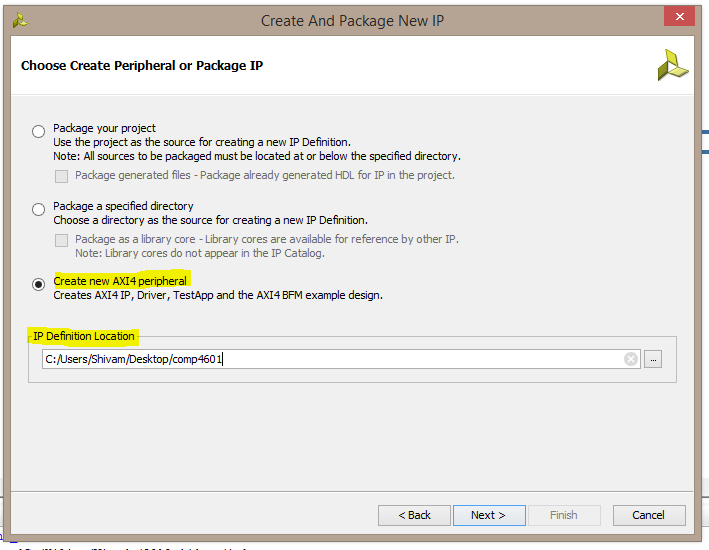
# Create custom IP

We will now go through the steps to generate your own custom AXI-LITE IP.

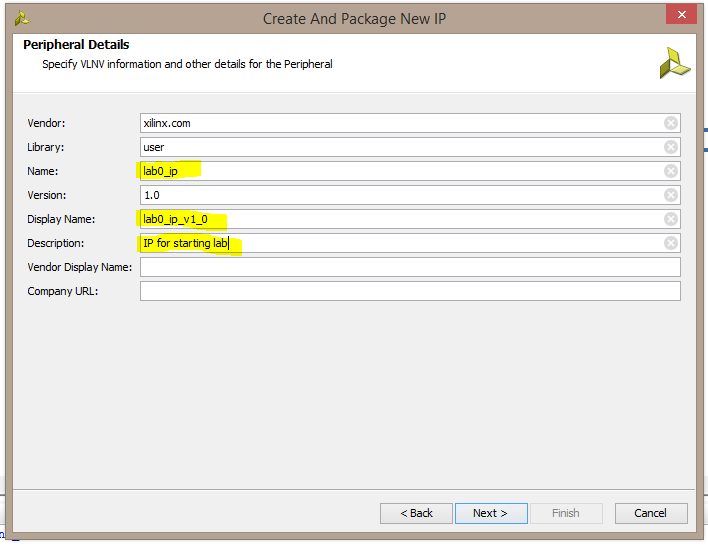
1. Go to the tools menu and select “Create and Package IP”
2. On the first screen select the next option



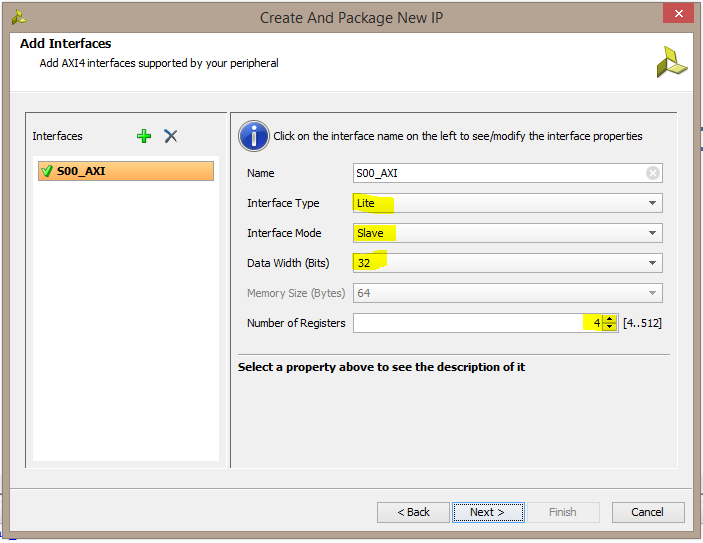
1. Select “Create new AXI4 peripheral” and then in the IP location, go up one directory from where your high level project file is located; so your high level project directory and IP that we are creating will sit in the same directory (e.g. C:/…./XX/high\_level\_proj & C:/…/XX/IP\_proj)



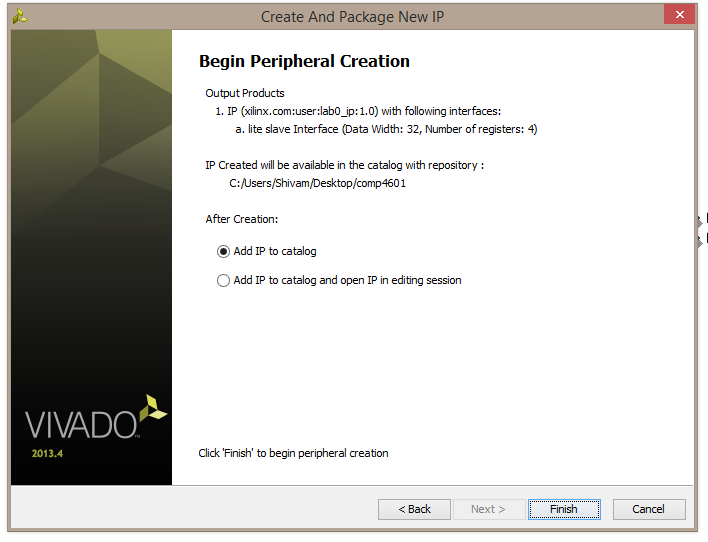
1. Feel free to provide whatever name you choose for the IP name, we have named it “lab0\_ip”, just make sure you update the display name accordingly, and update the description to whatever you feel.



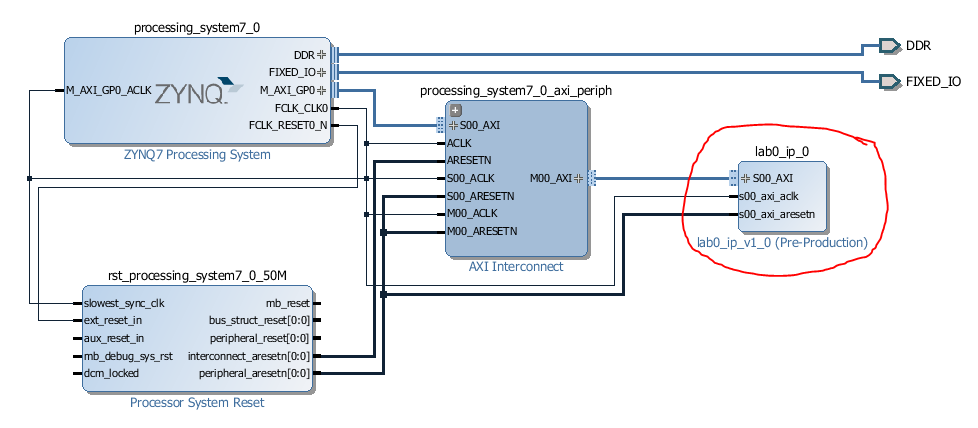
1. For the next menu we’ll keep the default options selected, here is an explanation as to why those options were selected:
   1. LITE – Simplest of the three AXI protocols to program for, Full AXI allows for burst (4 packet at a time) transfer, while Stream offers continual data transfer, however both Full & Stream feature poor driver support, hence we will stick to LITE at this time.
   2. Slave – Since this IP is going to be issued commands by the processor this IP will act as a slave
   3. 32 bits – Again for simplicity, keeps the bus sizes manageable
   4. 4 registers – This option will affect the generated AXI code, with 4 registers the data transferred from Master to Slave will be stored in 4 unique registers, the lower 4 bits act as a multiplexing address (byte addressed, b0000 first register, b0100 second register, b1000 third register and b1100 fourth register, hence the MSB’s of the address are not utilised for a 4 register design)



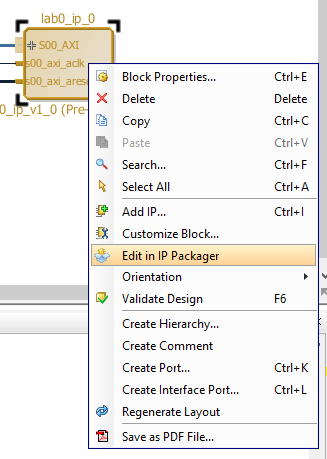
1. Leave the two options unchecked (Generate drivers/AXI4 BFM simulation example) and select next.
2. Leave “Add IP to catalog selected” and click finish



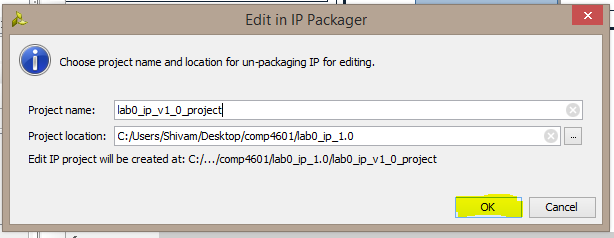
1. In the block diagram with the Zynq processor only, select “Add IP” and find the IP that you just named and created.
2. Select the “Run connection automation” to the s00\_AXI of the custom IP just created, the end result should be as follows:



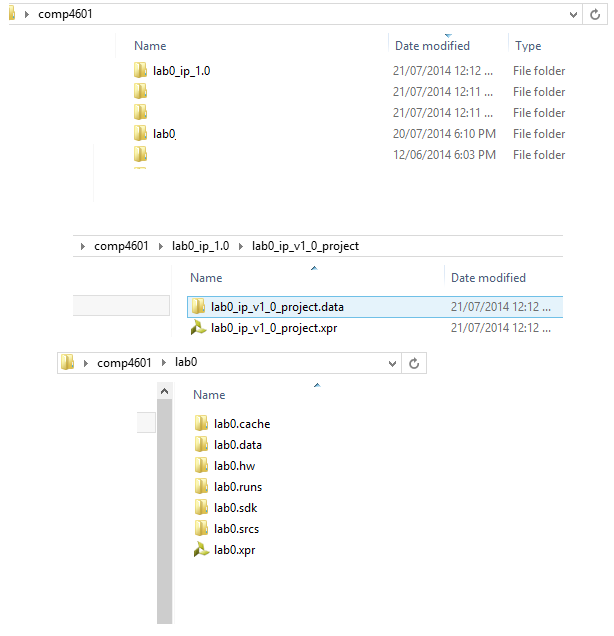
* 1. Now save your block design and/or project file
  2. Now right click the IP block in your design and select “Edit in IP Packager”



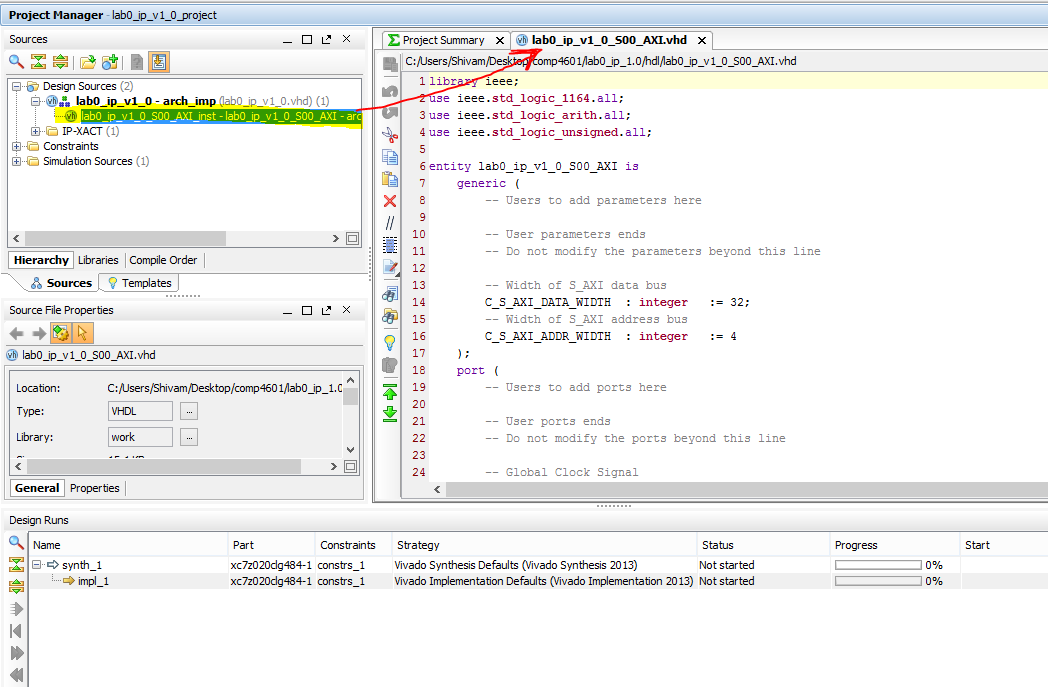
* 1. Select “Ok” in the project location screen



* 1. When the new instance of Vivado shows up the first thing to do is to close it. The reason for this is so that a permanent project file will form.
  2. Here is a breakdown of what your directory structure should look like, where you now have two project files one for the high level module (lab0) and the second which contains just the IP file (lab0\_ip\_1.0).



* 1. Now go to the lab0\_ip\_1.0/ lab0\_ip\_v1\_0\_project and open up the .xpr file shown above. (i.e. open up the Vivado project file for the custom IP). This should be close to an identical view of “edit in IP packager” which we temporarily saw before.
  2. Now open up the VHDL file called “lab0\_ip\_v\_1\_0\_S00\_AXI.vhd”, it show up in the project view



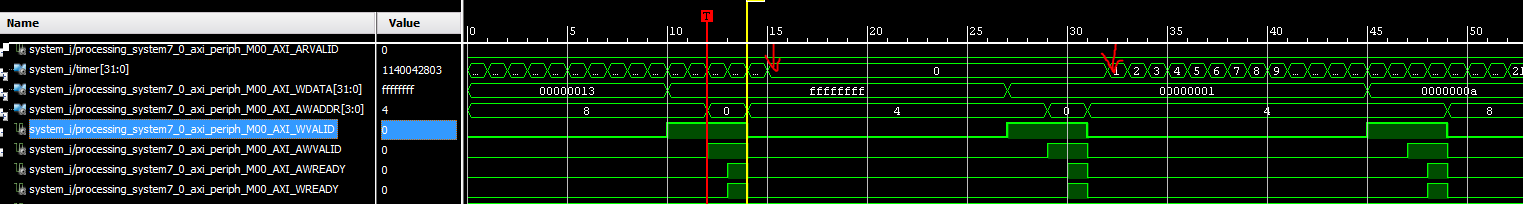
# AXI tutorial

We will now be making slight alterations to the stock provided S00\_AXI (Slave AXI implementation) so that it can better suit our needs, however prior to that we’ll go through the generated file by explaining how the AXI LITE protocol works and is implemented by the generated design. Advanced eXtensible Interface (AXI) is a protocol developed by ARM which is a mechanism for controlling shared bus access which is incredibly simple; some of the key features of this protocol are as follows:

* Separates address, control and data lines
* Burst mode transfer supported with the provision of only a starting address
* Uses a Master Slave model, with the Master directing the writes to the Slave and requesting reads of data from the Slave
* See [2] for full documentation of the AXI protocol

The Master accesses the slaves via addresses (each slave has a predefined range of addresses) and it is generally the Slaves responsibility to check the address to ensure that is addressing the individual slave and then assert the necessary signals on the bus lines, so that the data is transferred. However if you notice when you run connection automation on your custom AXI IP, Vivado inserts an AXI Interconnect in between the real master (Processor) and the Slave IP. See [3] for documentation on the implementation of the interconnect, but essentially it does most of the heavy lifting on arbitration and implementing a bus like nature through multiplexers and routing data embedded internally to the interconnect. The implication of this is that the Slave and Master AXI components can be significantly simplified such that they do not have to check addresses on the bus, and once the ready/valid signals are asserted for a particular slave it does not have to re-check addresses. This further builds abstraction allowing simpler and more generalised slaves (variable addresses) to be connected to Master components, the downside of this is that this introduces some delay (which will be seen in the timing diagrams below) due to the internals of this component [3].

## 2.a AXI Writes



The above waveforms show the master writing 0xFFFFFFFF @ BASE\_ADDR (0x0) then 0x00000001 @ BASE\_ADDR, and finally 0x0000000a @ BASE\_ADDDR+4 (0x4).

How AXI WRITES work:

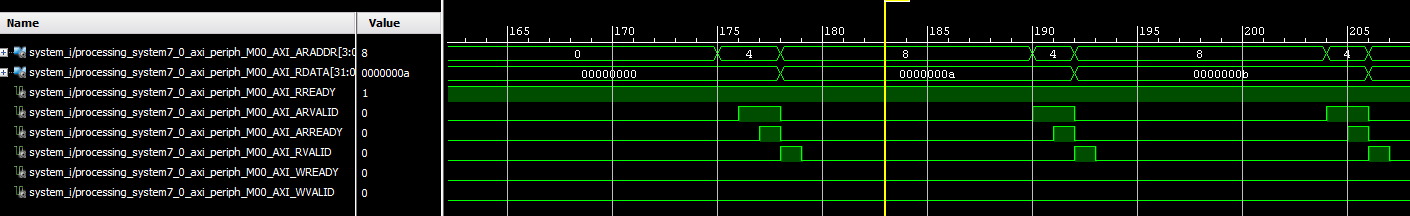
1. Master\* asserts WVALID (write data is valid, we can see that it is asserted the clock cycle 0xffffffff the data to be written is seen on WDATA)
2. Master\* asserts AWVALID (master asserting that it has placed the valid address on the address bus, seen on AWADDR becoming 0)

\*By Master Asserts – strictly speaking it is the AXI interconnect which acts as the master for this slave AXI component.

Slave then does the following:

1. Asserts AWREADY (write address can be accepted by the slave, determined by WVALID && AWVALID)
2. Asserts WREADY (write data can be accepted by the slave, determined by WVALID && AWVALID)
3. Also the write address is also latched (stored)
4. Once WVALID & AWVALID & AWREADY & WREADY are all asserted
   * Slave write is enabled
   * Next clock cycle (14cc in diagram, yellow line) the slave register (slv\_regX) has data on WDATA bus written into it
   * Because our timer implementation reads the slave register value on the rising edge the next clock cycle (15th clock cycle) it realises the value is 0xFFFFFFFF the trigger value to reset the timer, and we can see the timer being reset here

## 2.b AXI Reads



In the above example the processor is reading from a fifo which contains the data {0x0a, 0x0b, 0x0c, …..} from the custom IP via AXI-LITE at the address of BASEADDR+4.

For AXI Reads there are 4 basic signals to worry about:

1. Master pretty much always has the signal RREADY asserted, signalling it is always able to receive requested data back from the slave
2. Master then places the address that it wants to read from onto the ARADDR bus and asserts ARVALID

The slave then performs the following:

1. Slave the firstly asserts ARREADY (to signal that the address can be accepted by the slave, determined by ARVALID only) and then is upon this signal that the
2. Slave then asserts RVALID upon which ARREADY is de-asserted and the read is completed by the master, at this point the correct read data is placed onto the bus, where it has a limited amount of time to be read by the master. The RVALID signal is then de-asserted exactly one clock cycle later.

Other signals which can be utilised but are not included in your own designs are:

* BRESP/RRESP – Write response/Read response: AXI allows for a return of value by the slave upon every write/read.
* BVALID & BREADY – used in the same nature the AXI read valid/ready signals are, with the master asserting the ready signal when it can accept a response (pretty much all the time) and the valid signal being asserted by the slave when there is valid data on the BRESP bus.

## 2.c Customising the custom IP

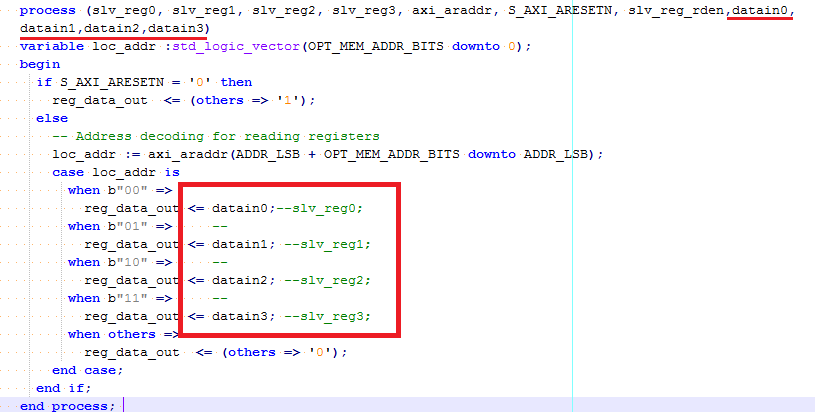
Based on the guide above about the AXI protocol above it should be clear that the signals can used by the programmer to determine whether or not a read/write has been placed by the master and to determine if certain actions on the slave should be undertaken. There are a number of ways to which this effect can be achieved, and we will introduce these by simple projects involving the implementation of a hardware timer, hardware FIFO and hardware GPIO which allow communication to the physical buttons and LED’s.

Firstly however there are some general modifications which will greatly speed up the design process, they are as listed in the following section. Just a couple of files and naming conventions to take a note of before starting:

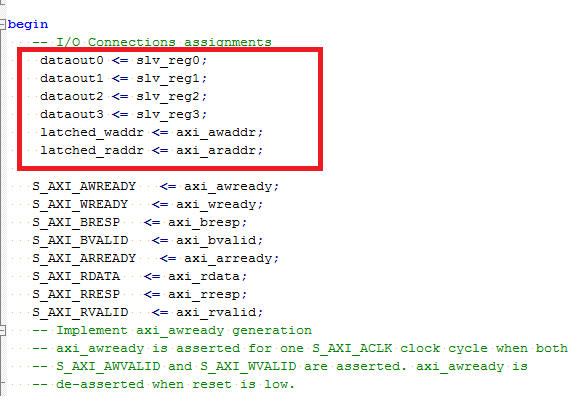
* “<your\_ip\_name>\_S00\_AXI.vhd” – generated file which implements the AXI-LITE handshaking process and stores all writes into registers, and uses those same registers as read response values.
* Toplevel refers to the toplevel VHDL file which encapsulates the AXI implementation file described above, you’ll notice that is largely empty, and is where we will be programming most of the code here. When coding your own designs it is recommended that you use this file as a connection point for your major sub VHDL components, however given this is a relatively small tutorial we will code entirely within this file for convenience.

### 2.c.i Changes to ‘\_S00\_AXI.vhd’

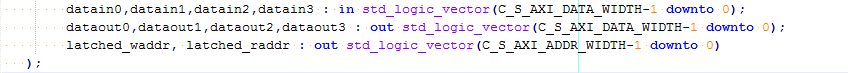
Firstly you should notice that the output values for the AXI reads are driven by reg\_data\_out, but these signals are originally being driven by the slave registers (which are the registers the AXI write data is stored into) since this is pointless we’ll replace it with our own signals (datain0/1/2/3) which will later be declared as inputs to the S00\_AXI component.



Now that we have taken care of the output values, we next need to worry about getting the AXI written values out of this component as well; hence we can simply pipe out these values (since they are all implemented as registers) out of this generated AXI component onto the toplevel where they can be used.



Notice from the timing diagrams in section 2.a/b that the address bus data is valid for a very short amount of time, hence the **axi\_awaddr/axi\_araddr** are used by the implementation as latches for the address, storing it for a single transaction (write or read respectively), hence we will need these values as well. As a consequence the following signals (image below) have to be added to the definition of the S00\_AXI component, so that the toplevel component can pipe in AXI read values, and the written values can be read by the toplevel.



### 2.c.ii Changes to Toplevel

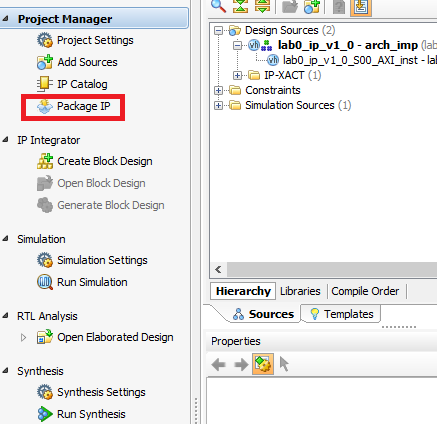
There are two ways in order to utilise the values from the processor:

* Firstly you can simply use the existing register implementation in the generated AXI protocol and read from the registers, if your implementation is not dependent on user actions and simply runs on its own based on the values the user has sent to you. While for AXI-reads static values can simply be inserted and read by the user on a needs basis.
* The second (much more useful approach) is to do this in real time while the reads/writes are taking place on the AXI bus so that you can effectively snoop the bus lines for data, thus being able to realise when the master has evoked an action and being able to react accordingly. Of course the actual AXI implementation can be modified to achieve this same goal, however to keep the complexity down to a minimum and prevent difficult to debug problems whereby the protocol has been implemented incorrectly we’ll describe the snooping based approach.

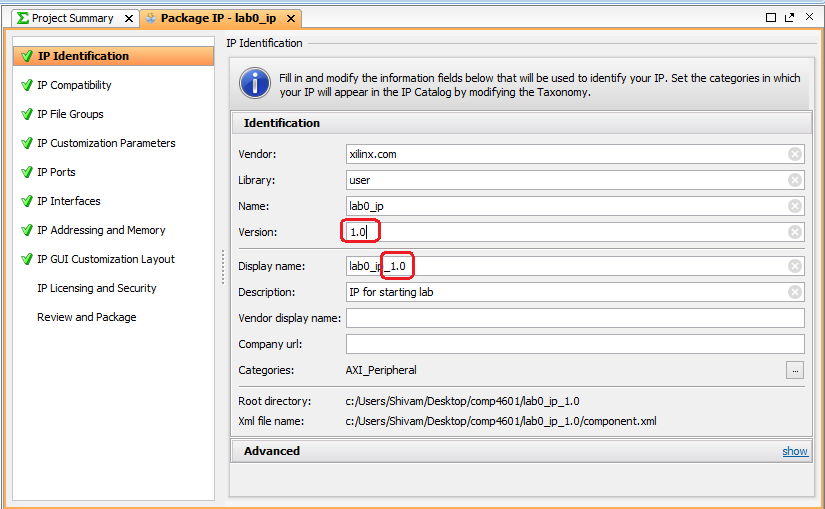
# Saving your IP

## 3.a IP Packager

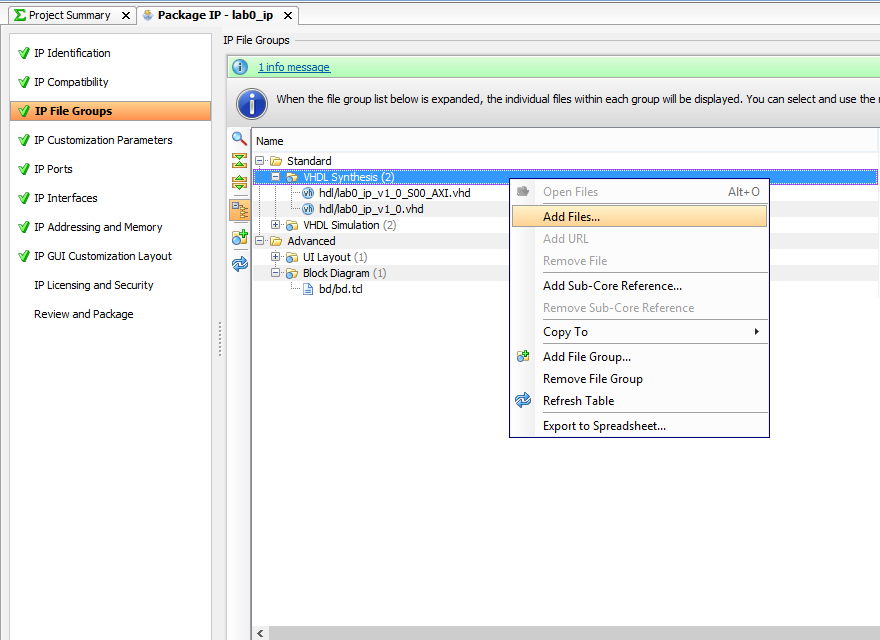
1. Once you are happy with your changes and have verified the syntax by running a synthesis of the IP, select the “Package IP” in the project manager section in the left hand pane.



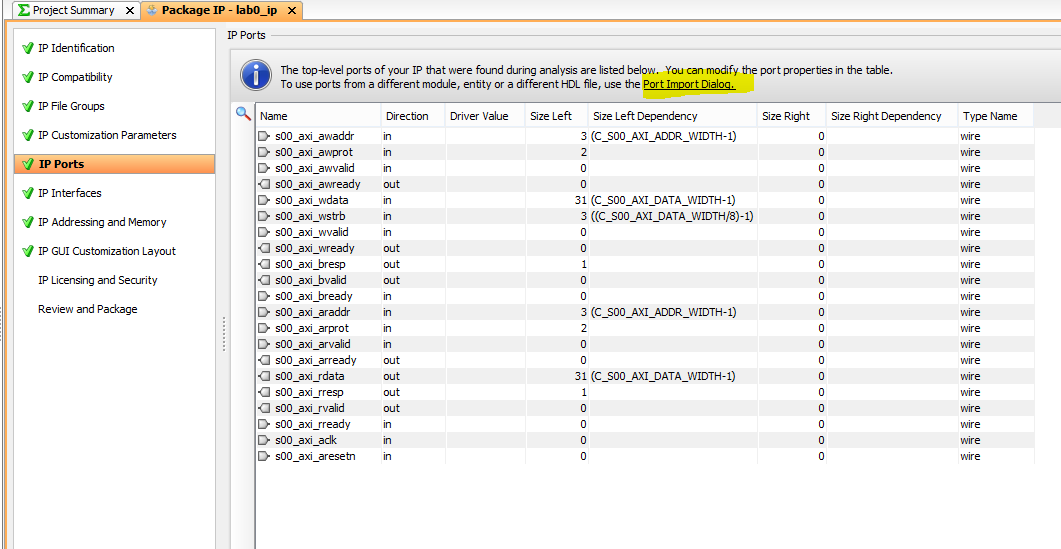
1. At the starting screen leave all the options the same except the version number; ensure that you **INCREASE** the version number (e.g. 1.0 -> 2.0). The reason for this is so that Vivado picks up on the changes, and prompts you for an upgrade. Also alter the display name to reflect the version increase.



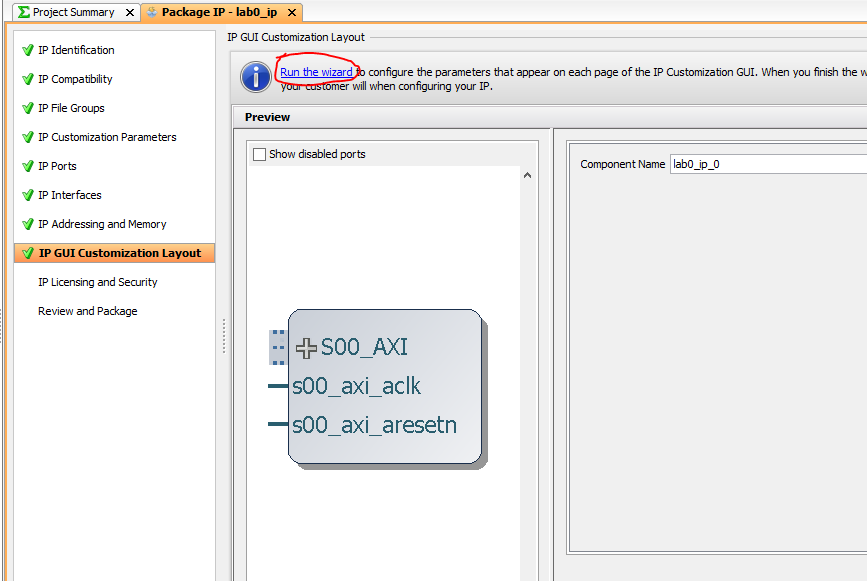
1. If the changes to the file involved adding new VHDL files, they must be added them in the **“IP File Groups”** to both the “VHDL synthesis” and “VHDL Simulation” folders, as shown by the diagram below.



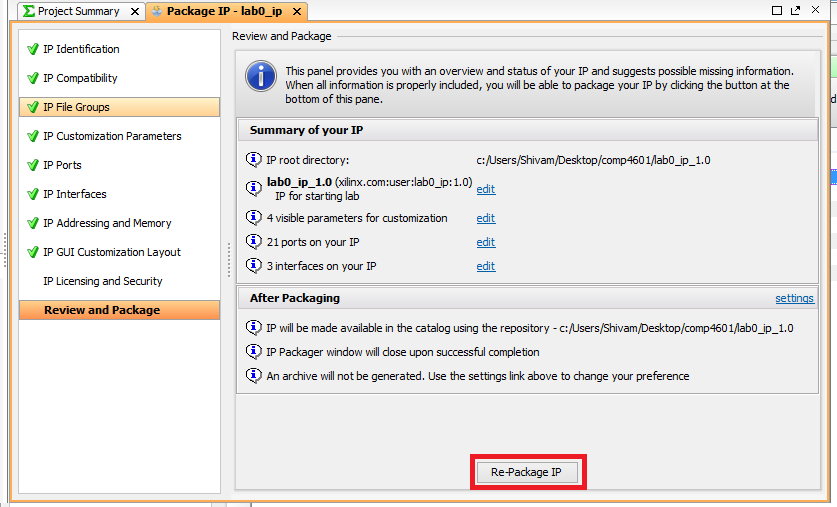
1. If the ports have been changed, then use the “**IP Ports**” page, simply clicking on the Port import dialog and follow the prompts.



1. If you used the “IP ports” page to add/remove ports, you should now go to the “**IP GUI Customization Layout**” and use the IP GUI customization layout wizard to regenerate the image of the IP component. Simply use the run the wizard link to regenerate the diagram of the IP.



1. To complete the process, in the “**Review and package”** screen select Re-Package IP



Screens which were skipped:

* **IP compatibility** - it is used to specify what boards the IP is valid for, which will always be the ZYNQ board for our designs.
* **IP Customisation Parameters** – should be used if the custom parameters (generic parameters) for the IP have been changed.
* **IP interfaces** – If the ports for the IP were changed and you wish to create a standardised port (e.g. you create a FIFO\_WRITE port that you want to connect to a Xilinx FIFO) then you can group ports together to create an IP interface.
* **IP Addressing and Memory** – Informational only
* **IP Licencing and Security** – Informational only

## 3.b IP upgrade in highlevel design

# Implementation Exercises

I’m thinking of walking through the implementations of the following components…

## 3.a Timer implementation

## 3.b FIFO implementation

## 3.c GPIO implementation

## 3.d Block ram implementation

Leave this as exercise, however provide the protocol to implement (and solution is provided).

References

[1] Xilinx custom IP guide, slightly outdated but quite comprehensive guide to custom IP

<http://www.xilinx.com/support/documentation/application_notes/xapp1168-axi-ip-integrator.pdf>

[2] AXI reference guide

<http://www.xilinx.com/support/documentation/ip_documentation/ug761_axi_reference_guide.pdf>

[3] Xillinx AXI Interconnect

<http://www.xilinx.com/support/documentation/ip_documentation/axi_interconnect/v2_1/pg059-axi-interconnect.pdf>